A1 polarity change of the electric driving signals, controlled by the comparator (20), are as small as possible.

7. (Amended) The electronic circuitry for the implementation of the driving scheme as claimed in claim 5, characterized in that it reduces the time-interval variations of the polarity change of the electric driving signals by using the additional analog switch (24), which selects between the voltage levels V_{S1} and V_{S2} connected to the inputs (27) and (28) of the said analog switch so that it changes the reference voltage V_C at its output (25) connected to the reference input (55) of the comparator (54) and

A2

that the selection of the reference voltage is made according to the signal given by the sensor element (35) and synchronized with the appropriate electric driving signal for the LCD electrooptic switching element (1) so that the signal that is generated by the sensor (35) at its output (34), connected to the synchronization input (31), synchronizes the logic control circuitry (30), which through its output (32), connected to the control input (26) of the analogue switch (24), controls the said analogue switch (24) in such a way that it selects the reference voltage V_C at its output (25), connected to the reference input (55) of the comparator (54), so that the time-interval variations of the polarity change of the electric driving signals, controlled by the comparator (54), are as small as possible.

8. (Amended) The electronic circuitry for the implementation of the driving scheme as claimed in claim 5, characterized in that the integration of the LCD electrooptic switching element driving signals is implemented by the periodic, sufficiently frequent, transfer of the charge proportional to the LCD electrooptic switching element driving voltage, into the integrating capacitor (110) by the transfer capacitor (101) and electronic analog switches (102) and (103), where the complete transfer of the charge from the transfer capacitor (101) into the integrating capacitor (110) is provided by two transistors of the opposite polarity (115) and (116) with base leads interconnected and emmitor leads interconnected.

9. (Amended) The electronic circuitry for the implementation of the driving scheme as claimed in claim 5, characterized in that the comparation of the integral of the LCD control signals with the reference voltage V_C and the discharging of the integrating capacitor (110) is provided by two transistors of the opposite polarity (117) and (118), which have their base leads connected to the collector leads of the other transistor, while remaining emitter leads are connected to the integrating capacitor (110) and the output signal from the circuit is provided by additional NPN transistor (119).

capacitor (101) and electronic analog switches (102) and (103), where complete transfer of the charge from the transfer capacitor (101) into the integrating capacitor (110) is provided by two transistors of the opposite polarity (115) and (116) with base leads interconnected and emmitor leads interconnected.

9. The electronic circuitry for the implementation of the driving scheme ~~of claim 1~~ as claimed in claims 5 ~~and 6,~~ characterized in that the comparation of the integral of the LCD control signals with the reference voltage V_C and the discharging of the integrating capacitor (110) is provided by two transistors of the opposite polarity (117) and (118), which have their base leads connected to the collector leads of the other transistor, while remaining emitter leads are connected to the integrating capacitor (110) and the output signal from the circuit is provided by additional NPN transistor (119).

Please add the following new claims:

10. (New) The electronic circuitry for the implementation of the driving scheme as claimed in claim 6, characterized in that it reduces the time-interval variations of the polarity change of the electric driving signals by using the additional analog switch (24), which selects between the voltage levels V_{S1} and V_{S2} connected to the inputs (27) and (28) of the said analog switch so that it changes the reference voltage V_C at its output (25) connected to the reference input (55) of the comparator (54) and

that the selection of the reference voltage is made according to the signal given by the sensor element (35) and synchronized with the appropriate electric driving signal for the LCD electrooptic switching element (1) so that the signal that is generated by the sensor (35) at its output (34), connected to the synchronization input (31), synchronizes the logic control circuitry (30), which through its output (32), connected to the control input (26) of the analogue switch (24), controls the said analogue switch (24) in such a way that it selects the reference voltage V_C at its output (25), connected to the reference input (55) of the comparator (54), so that the time-interval variations of the polarity change of the electric driving signals, controlled by the comparator (54), are as small as possible.

11. (New) The electronic circuitry for the implementation of the driving scheme as claimed in claim 6, characterized in that the integration of the LCD electrooptic switching element driving signals is implemented by the periodic, sufficiently frequent, transfer of the charge proportional to the LCD electrooptic switching element driving voltage, into the integrating capacitor (110) by the transfer capacitor (101) and electronic analog switches (102) and (103), where the complete transfer of the charge from the transfer capacitor (101) into the integrating capacitor (110) is provided by two transistors of the opposite polarity (115) and (116) with base leads interconnected and emmitor leads interconnected.

12. (New) The electronic circuitry for the implementation of the driving scheme as claimed in claim 6, characterized in that the comparation of the integral of the LCD control signals with the reference voltage V_C and the discharging of the integrating capacitor (110) is provided by two transistors of the opposite polarity (117) and (118), which have their base leads connected to the collector leads of the other transistor, while remaining emitter leads are connected to the integrating capacitor (110) and the output signal from the circuit is provided by additional NPN transistor (119).